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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,961	10/15/2001	Albert Lespagnol	Q66404	1041

7590 07/25/2005

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EXAMINER	
LE, VIET Q	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,961	LESPAGNOL, ALBERT	
	Examiner	Art Unit	
	Viet Q. Le	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/15/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozaki et al. (U.S. 5,365,519) hereinafter referred to as Kozaki.

Regarding claim 1, Kozaki disclosed a data packet switching node (Figure 1, switch 1) to be used in an asynchronous digital network, comprising:

An input stage (Figure 1, box 20), cutting data packets into segments of constant length (Figure 1, box 20, 300 Mb/sec is de-multiplexed down to 150 Mb/sec data streams),

A switching matrix for switching (Figure 1, switch matrix 1), said switching matrix having input ports (Figure 1, input ports Si0 to Si3) and output ports (Figure 1, output ports SoO to So3) supporting identical bit rates B (Bit rate of 150Mb/sec);

And an output stage reconstructing said data packets from said segments supplied by said output ports of said switching matrix (Figure 1, box 22, inputs coming from the switching matrix of 150 Mb/sec and combined to any higher rate. In this figure, the higher rate is 300 Mb/sec);

Wherein

Said input stage comprises at least one input interface with a bit rate equal to a multiple of B, ki*B, and means for splitting data packets received on said interface into segments distributed to ki input ports of said switching matrix (Figure 1, box 20 having 1 input port at rate of 300 Mb/sec which is 2 times the rate of the switching matrix of 150 Mb/sec. The de-multiplexer split the rate to 2 outgoing rates of 150 Mb/sec each to the switching matrix);

Said output stage comprises at least one output interface with a bit rate equal to a multiple of B, ko*B, and means for reconstructing a data packet with a bit rate equal to ko*B by concatenating segments supplied by ko output ports of said switching matrix (Figure 1, box 22 having 2 output ports coming out from the switching matrix at rates of 150 Mb/sec. The multiplexer combines these 2 rates of 150 Mb/sec to a output port of 300 Mb/sec which is 2 times the 150 Mb/sec rate); and

ki*ko> 1 (Figure 1, box 20 and 22. Ki = 2 and Ko = 2. Ki*Ko=2*2=4).

Regarding claim 2, Kozaki disclosed a data packet switching node according to claim 1, said switching matrix further comprising:

A first memory location for storing an identifier representing the association between said input interface and said corresponding ki input ports (Figure 2, box 104. Column 5, lines 61-68 & Column 6, lines 1-2);

A second memory location for storing an identifier representing the association between said output interface and said corresponding ko output ports (Figure 2, box 104; Column 6, lines 18-24).

Regarding claim 3, Kozaki disclosed a data pocket-switching node according to claim 1, said switching matrix further comprising:

A buffer memory for storing segments belonging to a packet received at said input interface (Figure 2, Buffer memory 11),

Memory writing means for sequentially writing segments received on said ki input ports in said buffer memory (Figure 2, Box 101);

A translation table for determining the output interface to which said segments belonging to said packet must be switched (Figure 2, Control table 104);

A traffic management module for storing the address of the first segment of said packet in said buffer memory (Figure 2, control table 104 and Buffer 11; Column 5, lines 38-41);

Memory reading means for retrieving consecutive segments belonging to said packet in said buffer memory and cyclically assigning each of said segments to one of said ko output pods associated to said output interface (Figure 2, Buffer memory control circuit 10; Column 6, lines 18-38).

Regarding claim 4, Kozaki disclosed a data packet switching node according to claim 1, dedicated to be used in an ATM switch to switch fixed length data packets supplied on said input interface (Figure 1, switching unit 1; Column 4, lines 43-45).

Regarding claim 7, Kozaki disclosed a data packet switching node according to claim 2, wherein the association between each input interface and corresponding input ports, as well as the association between each output interface and corresponding output ports are dynamically configurable in said first and second memory location

(Figure 1, boxes 20, 21, 22, 23; Various different relationships between input ports and the switch input ports or output ports and the switch output ports can be arranged as long as the rate of the switch is operating at 150 Mb/sec).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5 & 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozaki in view of Prabhakar et al. (U.S. 6,351,466) hereinafter referred to as Prabhakar.

Regarding claim 5, Kozaki disclosed a data packet switching node switching at the same packet segment length (Figure 1, switch 1) to be used in an asynchronous digital network as described in claim 1 above.

Kozaki, however, fails to disclose a data packet switching node to be an IP router to switch variable length data packets.

Prabhakar disclose the switching system and method that are used in either ATM switches or IP router (Column 1, lines 6-12).

It would have been obvious to one having ordinary skills in the art at the time the invention was made to have an IP router that can route data packets at the same rate with input and output ports at higher rate using multiplexer and de-multiplexer devices,

the motivation being that using IP infrastructure of the IP router, the switch will be able to support IP packets.

Regarding claim 6, Kozaki, however, fails to disclose a data packet switching node used in an equipment providing both IP routing and ATM switching functions.

Prabhakar disclose the switching system and method that are used in either ATM switches or IP router (Column 1, lines 6-12).

It would have been obvious to one having ordinary skills in the art at the time the invention was made to have both an ATM switching functions and the IP routing functions that can route and switch data packets at the same rate with input and output ports, the motivation being that using an infrastructure supporting both IP routing and ATM switching function, the switch will be able to support IP routing packets and ATM switching function.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q. Le whose telephone number is 571-272-2246. The examiner can normally be reached on 8 AM -5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VL

CHI PHAM
SUPERVISORY PATENT EXAMINE
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7/22/05